continuation of U.S. Pat. 5,424,881, issued 6/13/95, both of which are hereby incorporated by reference in their entireties.

Please insert the following new paragraph at page 12, line 22:

Figure 7 is a state transition diagram for a sequence detector matched to a trellis code (RLL d=I constraint).

AMA 4/9/05

Please delete the paragraph beginning at line ~~3~~ 23 on page 13.

Please replace the paragraph beginning at line 23 on page 14 with the following rewritten paragraph:

Figure 3 provides a block diagram illustrating the general organization of the CL-SH4400. As may be seen in Figure 3, the digitized read data for the CL-SH4400 is provided in an N-bit parallel form as digitized read data DRD0 and DRD1. Each of these two signals in the preferred embodiment disclosed is a 6-bit digitized read data signal. These two N-bit signals represent digitized samples of a read signal directly from a read head of the storage device after analog amplification and analog filtering. Those skilled in the art will recognize that the purpose of the analog amplifier and the analog filter is to scale the signals to the input range of the digital to analog converter and to attenuate frequencies above the Nyquist frequency (1/2 the sample frequency) to avoid signal distortion due to aliasing. In general, the analog filter will perform pulse shaping as well. The digitized read data signal DRD0 is a digitized read signal sample effectively taken near the center of a channel bit time (defined by the VFO frequency), subject however to a small amount of timing error or intentional timing set point offset in the VFO. The

pulse. Hence the read channel can be more suitably matched to the storage medium to provide better performance.

AMA 4/9/08

Please insert a new paragraph beginning at line ~~12~~ 21 on page 31 as follows:

The state machine model for the partial response sequence detector **40** is shown in Figure 7. Note that the model embodies several kinds of information. First, the isolated pulse sample values a, b, 1, and c are included. Second, the alternating polarity of pulses constraint is enforced. Third, the minimum run-length constraint of d=l is enforced; that is, the state transition diagram is matched to a trellis code constraint.

Please delete the paragraph beginning at line 11 on page 34:

Please delete Appendices 1, 2, 3, 4 and 5.